

*Sub C 33*

4 a plurality of basic cells regularly arranged on said  
5 semiconductor substrate;

6 a plurality of field effect transistors arranged in  
7 each of a plurality of said basic cells and formed in said  
8 semiconductor region;

9 power supply wirings arranged for supplying the power  
10 supply voltages to a plurality of said field effect  
11 transistors; and

12 switch elements provided between said semiconductor  
13 region and said power supply wirings,

14 wherein said switch elements include field effect  
15 transistors of said basic cells.

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Please cancel Claims 2-6 without prejudice or  
disclaimer.

*Sub C 33*

1 22. (Twice Amended) A semiconductor device as claimed  
2 in any one of claims 7 to 12, further comprising:  
3 a first wiring layer formed over said switch elements;  
4 a second wiring layer formed over said first wiring  
5 layer and having wiring extending in a direction transverse  
6 to wiring of said first wiring layer; and  
7 a third wiring layer formed over said second wiring

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8 layer and having wiring extending in a direction transverse  
9 to wiring of said second wiring layer,  
10 wherein a wiring electrically connected to gate  
11 electrodes of said switch elements is formed of wiring of  
12 the third wiring layer and arranged in parallel to said  
13 power supply wirings.

*Cmt*  
*B2*

1 23. (Twice Amended) A semiconductor device as claimed  
2 in any one of claims 7 to 14, wherein a semiconductor  
3 region for power feeding to supply a predetermined voltage  
4 to the semiconductor region formed in said semiconductor  
5 substrate is formed in a region between an internal circuit  
6 region where a plurality of said basic cells are arranged  
7 and a peripheral circuit region at an external side of said  
8 internal circuit region.

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1 34. (Amended) A semiconductor device, comprising:  
2 a semiconductor region formed in a peripheral circuit  
3 region of a semiconductor substrate;  
4 a plurality of cells for input/output circuits  
5 regularly arranged in the peripheral circuit region of said  
6 semiconductor substrate;  
7 a plurality of field effect transistors for

8       input/output circuits arranged in each of a plurality of  
9        said cells for input/output circuits and formed in said  
10      semiconductor region;

11      power supply wiring arranged for supplying a power  
12      supply voltage to a plurality of said field effect  
13      transistors for input/output circuits; and  
14      switch elements provided between the semiconductor  
15      region in said peripheral circuit region and said power  
16      supply wiring,

17      wherein said peripheral circuit region includes an  
18      external region to arrange field effect transistors for  
19      input/output circuits of relatively higher threshold  
20      voltage and an internal region to arrange field effect  
21      transistors for input/output circuits of relatively lower  
22      threshold voltage, and

23      wherein said switch elements include field effect  
24      transistors not used for input circuit among the field  
25      effect transistors for input/output circuits in said  
26      internal region.

*Sb 33*   39. (Amended) A method of manufacturing a

*B4*   2    semiconductor device, comprising:

*B4*   3    (a) regularly allocating a plurality of basic cells on